

DECLARATION UNDER 37 CFR § 1.131(a)

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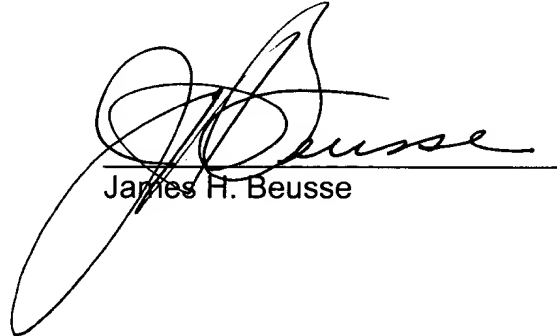
SEP-8 2003

TECHNOLOGY CENTER 2800

The undersigned, James H. Beusse, hereby declares that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon, declares as follows:

1. I am one of the named attorneys of record in the subject application.
2. The initial patent disclosure #122615 (attached as Exhibit A) that culminated in the subject application was sent to me on February 8, 2001 by the Assignee, Agere Systems, Inc. while I was a partner in the law firm of Holland & Knight, LLP.
3. At the time of receiving disclosure #122615, I had approximately 35 other patent disclosures from this same Assignee that were also being processed and the subject disclosure was placed in queue for processing.
4. During the time period of February-April 2001, I was actively discussing resignation from Holland & Knight and finally did resign as of April 30, 2001.
5. Part of the resignation process was to notify clients of my departure and to determine which projects would follow me and which would be retained by Holland & Knight.
6. Agere elected to have their files transferred to me after I had set up the new law firm of Beusse Brownlee Bowdoin & Wolter, P.A., effective May 1, 2001.
7. The turmoil arising from establishment of a new firm resulted in a slowing of the patent application preparation process so that the subject application was not filed until September 28, 2001 even though several attorneys were involved in preparing applications to reduce the backlog of cases being processed for this Assignee.
8. Despite the issues involved in resigning from one firm and starting another, we worked diligently to prepare and file patent applications on the numerous Agere disclosures.

9. In view of the activities occurring during the time period from February 8, 2001 until September 28, 2001, I believe that the delay of less than eight months between receipt of the disclosure and filing of the subject application demonstrates due diligence from a time prior to March 13, 2001 up to the filing date of the subject application.



James H. Beusse

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IP LAW USE	
Submission No	122615
Date Received	6/6
Attorney:	SMC

Title: A NOVEL BARRIER FOR CONTACT WINDOW AND VIA PLUGS.

Problem(s) addressed by the invention: Provide a new adhesion/barrier material for contact and via plugs that avoids issues with flaking and yield associated with TiN deposition.

Closest known solution: Frequent Ti pasting cycles when using TiN as a nucleation layer prior to W deposition.

DESCRIPTION OF THE INVENTION, keyed to drawings, sketches, photographs, etc., sufficient to enable one knowledgeable in the invention's field of technology to understand construction and operation of the invention.

Summary (30 words or less): Use of a graded barrier stack that avoids issues with frequent pasting, adhesion, stress and periodic flaking from chamber walls and chamber parts.

Detailed Description: Titanium nitride (TiN) thin films, deposited using PVD methods, has been used for a number of years in the prior art as a nucleation layer for contact window and via tungsten (W) plugs. Since TiN does not always adhere well to the window or via dielectric, the layer is almost always preceded by a deposition of a thin Titanium (Ti) adhesion layer. TiN films generate particles that limit yield of semiconductor devices. Intrinsic stresses in these TiN films cause these films to flake from the various parts of the PVD chamber, leading to particles, thus limiting device yield. Therefore, the deposition of TiN films necessitates frequent depositions of a Ti layer after every cassette of TiN processed wafers to reduce flaking and particle generation. This "pasting" of TiN chambers is time-consuming, costly and reduces fab cycle time and tool throughput. Furthermore, the TiN film has to possess good barrier qualities, because any pinholes in the layer will result in the WF_6 attack of the underlying Ti and cause a defect called "W-volcanoes".

Reduced feature sizes have prompted the industry to use newer PVD techniques such as ionized metal plasma (IMP) to improve Ti/TiN step coverage in the openings. With these depositions, bottom step coverage of about 50-60% is feasible for structures with opening dimensions of 0.18 micron diameter by 1 micron depth. The IMP process consists of TiN deposition from a Ti target as well as a Ti coil placed above the wafer. The process is well documented in the prior literature. Even with IMP processes, frequent Ti-pasting steps are necessary to prevent TiN flaking.

Therefore, what is needed in the art is a novel barrier stack for W-plugs that will prevent frequent pasting of chambers, improve yield by limiting particle generation, provide barrier integrity and serve as a nucleation layer for W-plugs.

The present invention requires the use of a novel barrier deposited from a composite source consisting of a WSi_x target and a W coil to serve as a nucleation and barrier layer for W plugs. The target and coil are fabricated using techniques well known in the prior art. Since it is difficult to fabricate a coil from WSi_x , the present invention requires a W coil. The combination of WSi_x and W materials allows the fabrication of a multilayered barrier material with a W-based compositional gradient across the barrier itself. The deposition is carried out such that the target first sputters WSi_x onto the wafer, then W is sputtered from the coil. This W layer serves as an excellent nucleation layer for the subsequent deposition of CVD-W to form W-plugs. The graded barrier allows good adhesion of WSi_x to the walls of the opening in the dielectric and the W serves as a nucleation layer for CVD-W. In another embodiment of the present invention, the deposition can be completed by yet another layer of WSi_x on top of the IMP-W deposited from the coil. Thus selectively switching the target and coil on and off in successive processing steps helps create this barrier. The coil is operated such that there is net erosion from the coil rather than deposition of WSi_x .

Advantages: Use of existing PVD equipment to deposit novel barrier stack by changing target and coil. Because all layers are essentially W-based, there is very good misfit between the various layers, resulting in low overall intrinsic stresses. Moreover, the problem associated with flaking from the walls of the chamber can be avoided by tailoring the WSi_x/W or $WSi_x/W/WSi_x$ depositions, so that the overall stress is essentially zero. The frequent pasting cycles required for TiN depositions are thus avoided, leading to improved cycle time and lower processing costs.

Commercial product(s) or other application in which the invention may be used: All IC chips with W plugs.

EXH. A



INTELLECTUAL PROPERTY LAW
FACSIMILE TRANSMITTAL SHEET

To: Jim Beusse

From: F. Romand

Fax: 244-5288

Pages: 2 (Including Cover Sheet)

Re: Bobby Blownik

Date: 2/8/01

☐ Urgent! ☐ For Review ☐ Please Comment ☐ Please Reply

• Comments:

Per discussion.

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EXH. B